ALARM MECHANISM

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to commonly assigned, co-pending U.S. Application Serial No. 09/334,431, entitled "CLIENT/SERVER ARCHITECTURE FOR A TELECOMMUNICATIONS NETWORK" and filed on June 16, 1999.

TECHNICAL FIELD

The present invention relates generally to the field of electronic circuits and, in particular, to alarm mechanisms for reporting alarm states and changes in alarm states.

BACKGROUND

Electronic equipment often includes circuitry that monitors the operation of the electronic equipment. This circuitry typically generates alarms when the equipment is not operating within normal parameters. For example, telecommunications equipment often includes circuitry that determines whether lines associated with a line card are operating properly. Such alarm mechanisms typically include software and hardware components that operate together to report alarm conditions.

In one conventional approach, the hardware component of the alarm mechanism indicates when an alarm changes from a first state, e.g., a non-alarm state, to an alarm state by an interrupt to the software component. Unfortunately, in this mechanism, the hardware typically does not provide an indication when an alarm changes from an alarm state back to a non-alarm state. Thus, the software typically polls the hardware on some recurring basis or uses some other mechanism to determine state changes back to the first or non-alarm state. This imposes an extra burden in developing the software code for the electronic equipment.

In other approaches, the software component of the alarm mechanism maintains an image of the current state of each alarm. When the hardware component indicates that an alarm has changed states, e.g., via an interrupt, the software component reads the current state conditions from the hardware and compares the current states with the

image maintained in the software component to determine which alarm changed states. Unfortunately, this approach also requires a significant burden on the software to obtain the needed information since the software component has to maintain and process the current state information each time an interrupt is received.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an improved alarm mechanism for electronic equipment that readily provides alarm information.

SUMMARY

The above-mentioned problems with alarm mechanisms and other problems are addressed by embodiments of the present invention and will be understood by reading and studying the following specification. Embodiments of the present invention provide an alarm mechanism that uses hardware registers to provide software components with both the current state of the alarm indicators and whether one or more of the indicators has changed states.

More particularly, in one embodiment an alarm mechanism is provided. The alarm mechanism includes a hardware component and a software component. The hardware component includes first and second registers. The first register is adapted to store a value that indicates a change in state of at least one alarm and the second register is adapted to store current states of each of the at least one alarm. The software component is responsive to interrupt requests from the hardware component and is adapted to read the first and second registers.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an embodiment of a telecommunications system including an alarm mechanism according to the teachings of the present invention.

Figure 2 is a block diagram of an embodiment of an alarm mechanism according to the teachings of the present invention.

Figure 3 is a flow chart that illustrates an embodiment of a process for an alarm

mechanism according to the teachings of the present invention.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

Figure 1 is a block diagram of an embodiment of a telecommunications system, indicated generally at 100, including an alarm mechanism according to the teachings of the present invention. The alarm mechanism is implemented in a plurality of multimedia channel banks 102-1, . . ., 102-N of access network 105. Multimedia channel banks 102-1, . . ., 102-N each include a plurality of line cards such as Plain Old Fashioned Telephone Service (POTS), Digital Subscriber Line (DSL) and Integrated Digital Services Network (ISDN) line cards. In one embodiment, the alarm mechanism monitors the states of a plurality of alarms of the multimedia channel bank. For example, the alarm mechanism in one embodiment monitors the states of a plurality of alarms associated with serial low voltage differential signal (LVDS) lines on the backplane of the multimedia channel bank or other access device. In this embodiment, an alarm state is generated when successive cells of the serial line include corrupted synchronization patterns. The successive cells may comprise actual data or idle cells. In other embodiments, the alarm mechanism monitors a plurality of alarms in an access device such as a dgital loop carrier. In other embodiments, the alarm mechanism monitors the state of other alarms associated with other aspects of the access device.

Access network 105 couples multimedia channel banks 102-1, . . ., 102-N with multimedia resource manager 104 and gateway module 108. Gateway module 108 provides connection to one or more networks 110, e.g., the Public Switched Telephone

Network (PSTN), the Internet, or other appropriate telecommunications network. An example of an access network 105 is shown and described in commonly assigned, co-pending application serial no. 09/334,431, entitled "CLIENT/SERVER BASED ARCHITECTURE FOR A TELECOMMUNICATIONS NETWORK" filed on June 16, 1999 (the "' 431 application"). The '431 application is incorporated by reference.

In one embodiment, multimedia channel banks 102-1, . . ., 102-N each include a hardware component and a software component that work together to provide a multi-register alarm mechanism. In one embodiment, the hardware component of the alarm mechanism includes first and second registers. The first register is adapted to store a value that indicates when an alarm of the multimedia channel bank changes states at least once, e.g., a selected alarm changes from an alarm state to a non-alarm state or from a non-alarm state to an alarm state. The second register is adapted to store current states of each of the alarms for the multimedia channel bank.

In operation, the multi-register alarm mechanism of, for example, multimedia channel bank 102-1, monitors the status of a plurality of alarms. When an alarm of multimedia channel bank 102-1 changes states, the fact that the alarm changed states is recorded in the first register of the hardware component of the alarm mechanism. For example, a bit in the first register is set to a high logic value to indicate that the state of the associated alarm has changed. Further, the current state of the alarm is recorded in the second register of the hardware component. For example, a bit in the second register associated with the alarm is set to a high logic value for an alarm state or a low logic value for a non-alarm state. Upon the change in states, the hardware component interrupts the software component to provide the updated information to the software component. In this manner, both the current state of the alarms of multimedia channel bank 102-1 and an indication of which of the alarms have changed states at least once is provided to the software for use in managing the operation of the multimedia channel bank 102-1.

Figure 2 is a block diagram of an embodiment of an alarm mechanism, indicated generally at 200, according to the teachings of the present invention. Alarm mechanism 200 includes hardware component 204 and software component 206. Alarm mechanism

200 receives information from monitored equipment via monitoring circuit 202. Hardware component 204 includes first and second registers 208 and 210. In one embodiment, each of the bits of first register 208 corresponds to a serial low voltage differential signal (LVDS) line on a backplane of an access device of a telecommunications network. In other embodiments, each bit in first register 208 is associated with a selected alarm of an electronic circuit. First register 208 stores a value in each bit location that indicates whether an associated alarm has changed states since the last reading of first register 208. In the example shown in figure 2, the alarms associated with bits 4 and 6 of first register 208 have changed states as indicated by the high logic value stored in these bit locations in the row labeled "CHANGE". Further, the alarms associated with bit locations 0-3, 5, and 7 have not changes states as indicated by the low logic levels stored in these locations.

Second register 210 also is a multi-bit register with each bit associated with a selected alarm, e.g., an alarm for a serial line on the backplane of an access device of a telecommunications network. Each bit in second register 210 stores the current state of each monitored alarm. In the example shown in figure 2, the alarms associated with bit places 4 and 7 are shown as being in an alarm state, e.g., as indicated by a high logic value, and the remaining bit locations 0-3, 5 and 6, are shown as being in a non-alarm state, e.g., as indicated by a low logic value.

In operation, software component 206 and hardware component to 204 function together to monitor the states of various alarms. Monitoring circuit 202 monitors the operation of the equipment. When an alarm condition changes, this information is reported to hardware component to 204 by monitoring circuit 206. The changed alarm condition is recorded in first and second registers 208 and 210, respectively. Namely, the current state of the alarm is recorded in a bit location in second register 210 associated with monitored alarm. Further, an indication is stored in the corresponding bit location of first register 208 to indicate that the associated alarm has changed states. Once the bit location in first register 208 indicates a change in states for a selected alarm, this value remains unchanged even in light of further changes to the state of the alarm until such time that the value is read by the software component. When a change

in states is detected, and information is recorded, an interrupt notifies the software component 206 such that software component 206 reads the values in first register 208 and second register 210.

Figure 3 is a flow chart that illustrates an embodiment of a process for an alarm mechanism according to the teachings of the present invention. The method begins at 302 and monitors the operation of electronic equipment, e.g., serial low voltage differential signal (LVDS) lines on a backplane of an access device in the telecommunications network. At block 304, the method determines whether an alarm condition exists. If not, the method returns to block 302. If however, the method determines that an alarm condition exists, the method proceeds to block 306.

At block 306, an alarm is generated. Further, at block 308, the method records a change in state of the alarm in a first register. For example, when an alarm changes from a non-alarm state to an alarm state, a high logic value is recorded in the bit location of the first register associated with the alarm. Similarly, when the alarm changes from an alarm state to a non-alarm state, a high logic value is also recorded in the bit location of the first register associated with the alarm. Once a bit location is changed to a high logic level, the bit value does not change until it is read by a software component and reset to a low logic value.

At block 310, the method records the state of the alarm in a second register. For example, the method records a high logic value for an alarm in an alarm state and a low logic value for an alarm in a non-alarm state. At block 312, the method generates an interrupt to the software component of the alarm mechanism indicating that a change in state has been recorded by the hardware component.

Conclusion

Embodiments of the present invention have been described. The embodiments provide an alarm mechanism having both a hardware component and a software component. The hardware component includes at least first and second registers. The first register stores an indication of a change in state of at least one alarm monitored by the alarm mechanism. The second register stores the current state of the alarms

monitored by the alarm mechanism. The values in these registers are read by software based on an interrupt from the hardware.

Although specific embodiments have been illustrated and described in this specification, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, embodiments have been described in terms of an alarm mechanism for an access device in a telecommunications network. It is understood, however, that the alarm mechanism described is not limited to use in an access device for a telecommunications network. Rather, the alarm mechanism in other embodiments is used in other appropriate electronic equipment. Further, the alarm mechanism is not limited to use in monitoring serial lines on a backplane of an access device. The alarm mechanism in other embodiments monitors other alarms in other electronic equipment. Further, the logic levels for the bits of the first and second registers in other embodiments are inverted from the embodiments described here.